Linxiao Shen

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Research Interests

- My Ph.D. work consists two contributions: ultra-high power-efficient OTA using inverter-stacking topology, ultra-area-efficient SAR ADC topology that breaks the fundamental kT/C thermal noise limit.

- My research interests of my ongoing and future research is in developing integrated circuit solutions to address the key challenges in all kinds of sensor interface systems (e.g. higher power efficiency circuit techniques), smarter IoT devices (e.g. AI-assisted edge-computing), and next-generation AI (e.g. analog and mixed-signal computing).

Education Background

08/2014 - present The University of Texas at Austin, Austin, Texas, USA
- Ph.D student in Prof. Nan Sun's research group

08/2010 - 06/2014 **B.Eng.** in Fudan University, Shanghai, China
- Ranked 1st and Graduated with the highest honor
- Thesis: Implanted glucose sensor readout circuit design

Awards & Scholarships

12/2018	**IEEE Solid-State Circuit Society (SSCS) Predoctoral Achievement Award**
06/2014	Outstanding undergraduate thesis award
06/2013	Top-10 excellent student awards in Fudan University
06/2012	National scholarship (top 1%) from Ministry of Education of China
06/2011	Samsung fellowship

Publications & Patents

Peer-reviewed Journals

[J1]. Linxiao Shen, Nanshu Lu, and Nan Sun, "A 1-V 0.25-uW Inverter Stacking Amplifier With 1.07 Noise Efficiency Factor,'' *IEEE Journal of Solid-State Circuits*, vol. PP, no. 99, pp. 1-10

Peer-reviewed Conferences

[C1]. Linxiao Shen, Nanshu Lu, and Nan Sun, "A 1V 0.25uW Inverter-Stacking Amplifier With 1.07 Noise Efficiency Factor,'' *2017 Symposium on VLSI Circuits*, Kyoto, 2017, pp. C140-C141.

[C2]. Hyoyoung Jeong, Taewoo Ha, Irene Kuang, Linxiao Shen, Zhaohe Dai, Nan Sun, and Nanshu Lu, ''NFC-Enabled, Tattoo-Like Stretchable Biosensor Manufactured by 'Cut-and-Paste' Method,'' *2017 39th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC),* Seogwipo, 2017, pp. 4094-4097.

[C3]. Yi Zhong, Shaolan Li, Arindam Sanyal, Xiyuan Tang, Linxiao Shen, Siliang Wu, and Nan Sun, ''A Second-Order Purely VCO-Based CT ΔΣ ADC using a Modified DPLL in 40nm CMOS,'' *2018 IEEE Asian Solid-State Circuits Conference (A-SSCC),* Tainan, 2018, pp. 93-94.

[C4]. Linxiao Shen, Yi Shen, Xiyuan Tang, Chen-Kai Hsu, Wei Shi, Shaolan Li, Wenda Zhao, Abhishek Mukherjee, and Nan Sun, ''A 0.01mm^2 25uW 2MS/s 74dB-SNDR Continuous-Time Pipelined-SAR ADC with 120fF Input Capacitor," accepted to *IEEE international Solid-State Circuits Conference (ISSCC), 2019, to appear*

[C5]. Xiyuan Tang, Shaolan Li, Linxiao Shen, Wenda Zhao, Xiangxing Yang, Randy Williams, Jiaxin Liu, Zhichao Tan, Neal Hall, and Nan Sun, "A 16fJ/conversion-step Time-Domain Incremental Zoom Capacitance-to-Digital Converter," accepted to *IEEE international Solid-State Circuits Conference (ISSCC), 2019, to appear*

[C6]. Biying Xu, Shaolan Li, Chak-Wa Pui, Derong Liu, Linxiao Shen, Yobo Lin, Nan Sun, and David Z. Pan, "Device Layer-Aware Analytical Placement for Analog Circuits," accepted to *IEEE International symposium of physical design (ISPD), 2019, to appear*

[C7]. Xiyuan Tang, Yi Shen, Linxiao Shen, Wenda Zhao, Zhangming Zhu, Visvesh Sathe, and Nan Sun, "A 10b 100MS/s SAR ADC with Reference Ripple Cancellation," accepted to *Custom integrated circuits conference (CICC), 2019, to appear*

[C8]. Shaolan Li, Wenda Zhao, Biying Xu, Xiangxing Yang, Xiyuan Tang, Linxiao Shen, Nanshu Lu, David Z. Pan, and Nan Sun, "A 0.025-mm^2 0.8-V 78.5dB-SNDR VCO-based Sensor Readout Circuit in a Hybrid PLL- ΔΣM Structure," accepted to

Custom integrated circuits conference (CICC), 2019, to appear
[C9]. Biying Xu, Yibo Lin, Shaolan Li, Linxiao Shen, Nan Sun, and David Pan, "WellGAN: Generative-Adversarial-Network-Guided Well Generation for Analog/Mixed-Signal Circuit Layout," accepted to *Design Automation Conference (DAC), 2019, to appear*

Under Review

[J2]. Hyoyoung Jeong, Liu Wang, Taewoo Ha, Ruchika Mitbander, Xiangxing Yang, Zhaohe Dai, Shutao Qiao, Linxiao Shen, Nan Sun, and Nanshu Lu, "Modularized Stretchable Electronic Tattoos with Wireless Power and Near-Field Communication Capabilities," submitted to *Small*
[J3]. Abhishek Mukherjee, Miguel Gandara, Biying Xu, Shaolan Li, Linxiao Shen, and Nan Sun, "A 1 GS/s 20 MHz-BW Capacitive-Input Continuous-Time ΔΣ ADC Using a Novel Parasitic Pole-Free Fully Differential VCO," submitted to *IEEE Solid-State Circuit Letter (SSC-L)*
[C10]. Linxiao Shen, and Nan Sun, "A 0.6-V Tail-Less Inverter Stacking Amplifier with 0.96 PEF and Chopping," submitted to *IEEE Symposium on VLSI Circuits (VLSI), 2019*
[C11]. Xiyuan Tang, Begum Kasap, Linxiao Shen, Wei Shi, and Nan Sun, ''A Floating Dynamic Comparator,'' submitted to *IEEE Symposium on VLSI Circuits (VLSI), 2019*

Patents

[P1]. Linxiao Shen, and Nan Sun, "Inverter stacking amplifier," US application number 62/514,684

Research & Projects

09/2015 - 06/2018 **Stretchable planar antenna modulation by integrated circuit (SPAMIC) for the near field communication (NFC) of epidermal electrophysiological sensors (EEPS)**

- Designed an ultra-low power action potential sensor readout low noise instrumentation amplifier (LNIA) with noise efficiency factor (NEF) of 1.07, **setting the world record**
- Designed an ultra-low voltage low-power chopper LNIA with power efficiency factor (PEF) of 0.97, **setting the world record**
- Optimized compensation method for multi-stage front-end amplifier specific for biomedical sensor readout

01/2018 - 10/2018 **Design of an extremely area efficient high-resolution Nyquist ADC**

- Designed a 13-bit SAR ADC with continuous-time operating kT/C noise-free first stage
- Occupied an active area of 0.0113 mm^2 in 40-nm CMOS process, achieving at least **5x smaller than state-of-the-art**
- **Break the fundamental kT/C limit** on minimally required sampling capacitance
- Relax the performance requirement of the ADC input/reference buffer, leading to significant power saving on the system level

03/2018 - present **Design of an adaptive continuous-time ΔΣ ADC with fast artifact recovery**

- Designed a CT ΔΣ ADC, whose quantization step is adaptively changeable to the input
- Relax linearity requirement of front-end integration with analog signal prediction and digital integration
- Achieved **105-dB dynamic range**

03/2018 - present **Design of a highly power efficient floating dynamic comparator**

- Achieved ultra-high common-mode rejection by using isolated power supply from a charged capacitor
- Realized **3.4x higher power efficiency** than conventional strong-arm comparator, with same input-referred noise performance

Work Experience

06/2018 - 08/2018 **Analog design intern, Silicon Laboratories, Inc**

- In charge of ultra-low power RC oscillator design for bluetooth communications

Teaching Experience

08/2017 - 12/2017 EE382M-14: Analog Integrated Circuit Design (Teaching Assistant)
02/2017 - 06/2017 EE382M-24: Analog/Digital Data Converter (Teaching Assistant)
08/2016 - 12/2016 EE382M-14: Analog Integrated Circuit Design (Teaching Assistant)
02/2015 - 06/2015 EE438K: Analog Electronics (Teaching Assistant)